

Notice of References Cited	Application/Control No. 10/773,333		Applicant(s)/Patent Under Reexamination OKUMURA, HIROSHI	
	Examiner Johannes P. Mondt		Art Unit 3663	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,133,609	10-2000	Nakamura, Kenichi	257/347
	B	US-			
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	L	US-			
	M	US-			

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Wolf, S., "Silicon Processing in the VLSI Era", Volume 3 - The submicron MOSFET, Lattice Press, Sunset Beach, California (USA) (1995) (ISBN: 0-961672-5-3), pages 592-594.
	V	Computerized Translation of Nakamura, Osamu (JP 2003-017502 A) as previously and presently cited.
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.